CLAIMS

What is claimed is:

1. A voltage subtractor/adder circuit comprising:

a differential pair having first and second MOS transistors, gate electrodes of said first and second MOS transistors forming input terminals for receiving an input differential voltage, drain electrodes of said first and second MOS transistors forming output terminals for outputting a subtraction output signal, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal for addition output voltage; and

wherein the sum of currents flowing through said first and second MOS transistors increases in proportion to the square of said input differential voltage.

2. A voltage subtractor/adder circuit as set forth in claim 1, further comprising a level shifter for level-shifting said addition output voltage from said source electrodes which are commonly coupled.

3. A voltage subtractor/adder circuit comprising:

a differential pair having first and second MOS transistors, gate electrodes of said first and second MOS transistors forming input terminals for receiving an input differential voltage, drain electrodes of said first and second MOS transistors forming output terminals for outputting a subtraction output signal, and source electrodes of said first and second MOS transistors being commonly coupled to form

an output terminal for addition output voltage; and

a constant current source which drives said differential pair.

4. A voltage subtractor/adder circuit as set forth in claim 3, further comprising a level shifter for level-shifting said addition output voltage from said source electrodes which are commonly coupled.

5. A MOS differential amplifier circuit comprising:

a MOS differential pair having first and second MOS transistors and receiving an input differential voltage, source electrodes of said first and second MOS transistors being commonly coupled and being driven by a current source; and

wherein current value of said current source being controlled such that a difference voltage between a common mode voltage and a common source voltage of said first and second MOS transistors becomes a constant value.

6. A MOS differential amplifier circuit as set forth in claim 5, further comprising a level shifter for level-shifting said common source volage of said first and second MOS transistors.

7. A MOS differential amplifier circuit comprising:

a MOS differential pair having first and second MOS transistors and receiving an input differential voltage, source electrodes of said first and second MOS transistors being commonly coupled and being driven by a constant current source; and

wherein a current is injected into said constant current

source such that a difference voltage between a common mode voltage and a common source voltage of said first and second MOS transistors becomes a constant voltage.

8. A MOS differential amplifier circuit comprising:

a MOS differential pair having first and second MOS transistors and receiving an input differential voltage, source electrodes of said first and second MOS transistors being commonly coupled and being driven by a constant current source; and

third and fourth MOS transistors which are load transistors of said first and second MOS transistors, respectively, and whose gates receive the sum of a predetermined constant voltage and a voltage obtained by subtracting a common source voltage of said first and second MOS transistors from a common mode voltage.

9. A complementary MOS differential amplifier circuit comprising:

a MOS differential pair having first and second MOS transistors and receiving an input differential voltage, source electrodes of said first and second MOS transistors being commonly coupled and being driven by a first constant current source;

a MOS quadri-tail cell having third, fourth, fifth and sixth MOS transistors which have different conductivity type from that of said first and second MOS transistors, source electrodes of said third, fourth, fifth and sixth MOS transistors being commonly coupled and being driven by a second constant current source;

wherein gate electrodes of said fifth and sixth MOS transistors being coupled to a common source electrode of said first and second MOS transistors, drain electrodes of said fifth and third MOS transistors being commonly coupled and forming one output terminal, drain electrodes of said sixth and fourth MOS transistors being commonly coupled and forming the other output terminal, and gate electrodes of said first and second MOS transistors and gate electrodes of said third and fourth MOS transistors receiving input voltages.

10. A complementary MOS differential amplifier circuit as set forth in claim 9, further comprising level shifters for level-shifting said input voltages before being applied to said gate electrodes of said first and second MOS transistors and said gate electrodes of said third and fourth MOS transistors.

11. A complementary MOS differential amplifier circuit as set forth in claim 9, wherein the ratio of the current value of said first constant current source and transconductance parameter of said first and second MOS transistors is approximately half of the ratio of the current value of said second constant current source and transconductance parameter of said third, foruth, fifth and sixth MOS transistors.

12. A complementary MOS differential amplifier circuit comprising first and second MOS differential amplifier circuits each of which is the MOS differential amplifier circuit as set forth in claim 6, wherein corresponding MOS transistors of said first and second MOS differential amplifier circuits have mutually different conductivity types and wherein said first

and second MOS differential amplifier circuits are coupled parallel to form a differential input pair.

13. A complementary MOS differential amplifier circuit as set forth in claim 9, wherein transconductance of said MOS differential amplifier circuit is adjustable by controlling current values of at least one of said first and second constant current sources.